



This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (cancelled) A semiconductor package for a micro-machined semiconductor device, comprising:

- a) a substrate having a first surface and a second surface, the micro-machined semiconductor device located adjacent the first surface;
- b) a plurality of vias, extending through the substrate between the first and second surfaces;
- c) an electrical connection located between the vias and the micro-machined semiconductor device for electrically connecting the vias to the semiconductor device;
- d) a solder seal, located between the micro-machined semiconductor device and the first surface for hermetically sealing the micro-machined semiconductor device;
- e) a rigid support located between the micro-machined semiconductor device and the first surface for supporting the micro-machined semiconductor device during assembly and preventing the micro-machined semiconductor device from contacting the first surface; and
- f) a plurality of solder spheres mounted to the second surface and electrically connected to the vias.

2. (cancelled) The semiconductor package according to claim 1, wherein the electrical connection includes:

- a) a first pad located on the micro-machined semiconductor device; and
- b) a second pad located on the first surface; and
- c) a solder joint connected between the first and second pad.

5 3. (cancelled) The semiconductor package according to claim 1, wherein the substrate is a low temperature co-fired ceramic.

4. (cancelled) The semiconductor package according to claim 1, wherein the seal is a ring of solder located adjacent an outer perimeter of the substrate.

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5. (cancelled) The semiconductor package according to claim 1, wherein the rigid support is attached to the first surface.

15 6. (cancelled) The semiconductor package according to claim 5, wherein the rigid support is gold.

7. (cancelled) The semiconductor package according to claim 5, wherein the rigid support is an alloy of gold and palladium.

20 8. (cancelled) The semiconductor package according to claim 5, wherein the rigid support is ultrasonically deposited.

9. (cancelled) The semiconductor package according to claim 3, wherein the substrate has a plurality of layers.

10. (cancelled) The semiconductor package according to claim 40 ~~9~~, wherein a plurality of circuit lines are located on the layers, the circuit lines connected between the vias.

11. (cancelled) The semiconductor package according to claim 1, wherein a ball pad is
5 attached to the second surface, the solder sphere attached to the ball pad.

12. (cancelled) The semiconductor package according to claim 11, wherein the solder sphere is attached to the ball pad by a reflowed solder paste.

13. (cancelled) A semiconductor package for a micro-machined semiconductor device comprising:

a) a low temperature co-fired ceramic substrate having a plurality of layers, the substrate having a top and a bottom surface;

5 b) a plurality of vias, extending between the layers;

c) a plurality of solder spheres, located on the bottom surface and electrically connected to the vias;

d) a plurality of rigid supports, attached to the top surface;

10 e) a solder seal located between the micro-machined semiconductor device and the top surface, the seal hermetically sealing the micro-machined semiconductor device;

f) the micro-machined semiconductor device spaced from the top surface by the rigid supports such that a movable portion of the micro-machined semiconductor device is unconstrained for movement, the rigid supports preventing the micro-machined semiconductor device from contacting the top surface during assembly; and

15 g) an electrical connection located between the vias and the micro-machined semiconductor device for electrically connecting the vias to the semiconductor device.

14. (cancelled) The semiconductor package according to claim 13, wherein the electrical connection includes:

- a) a first pad located on the micro-machined semiconductor device; and
- b) a second pad located on the top surface; and
- 5 c) a solder joint connected between the first and second pad.

15. (cancelled) The semiconductor package according to claim 13, wherein the solder seal is a ring of solder located adjacent an outer perimeter of the substrate.

10 16. (cancelled) The semiconductor package according to claim 13, wherein the rigid support is gold.

17. (cancelled) The semiconductor package according to claim 13, wherein the rigid support is an alloy of gold and palladium.

15 18. (cancelled) The semiconductor package according to claim 13, wherein the rigid support is ultrasonically deposited.

19. (cancelled) The semiconductor package according to claim 13, wherein a plurality of
20 circuit lines are located on the layers, the circuit lines connected between the vias.

20. (cancelled) The semiconductor package according to claim 13, wherein a ball pad is attached to the bottom surface, the solder sphere attached to the ball pad.

21. (cancelled) The semiconductor package according to claim 13, wherein the solder sphere is attached to the ball pad by a reflowed solder paste.

22. (previously withdrawn) A method of making a semiconductor package comprising

5 the steps of:

a) punching vias in at least two low temperature co-fired ceramic layers;

b) filling the vias with a conductor;

c) screen printing conductor lines on the layers;

d) screen printing a seal ring and a plurality of pads on one of the layers;

10 e) screen printing a plurality of ball pads on one of the layers;

f) stacking the layers;

g) laminating under pressure the layers into a substrate;

h) firing the substrate in an oven;

i) depositing a rigid support on the substrate;

15 j) screening a first solder paste onto the seal ring and the pads;

k) placing a micro-machined semiconductor device onto the substrate;

l) reflowing the first solder paste in an oven such that the micro-machined semiconductor device is attached to the substrate;

m) screening a second solder paste onto the ball pads;

20 n) placing a plurality of solder spheres onto the ball pads; and

o) reflowing the second solder paste in an oven such that the solder spheres are attached to the ball pads.

23. (previously withdrawn) The method according to claim 22, wherein the rigid support is an ultrasonically deposited metal.

24. (previously withdrawn) The method according to claim 22, wherein the metal is

5 chosen from the group consisting of:

a) gold; and

b) an alloy of gold and palladium.

25. (new) A semiconductor package comprising:

a planar low temperature co-fired ceramic substrate having a first and second layer mounted adjacent each other, the first layer having a first surface and the second layer having a second surface,

5 a micro-machined semiconductor device located adjacent the first surface, the micro-machined semiconductor device having a plurality of first pads and an active central area;

a plurality of ball pads located on the second surface;

a plurality of second pads located on the first surface;

10 a plurality of vias, extending through the substrate between the first and second surfaces, the vias connected to the ball pads and to the first pads;

a reflowed solder joint located between the first and second pads for electrically connecting the substrate to the semiconductor device, the reflowed solder joint formed from a first reflowed solder paste;

15 a solder seal ring, located between the micro-machined semiconductor device and the first surface around an outer perimeter of the substrate for making a hermetic seal between the micro-machined semiconductor device and the substrate;

a plurality of ultrasonically deposited wire bond bumps located between the micro-machined semiconductor device and the first surface for supporting the micro-
20 machined semiconductor device during assembly and preventing the micro-machined semiconductor device from contacting the first surface during reflow of the solder joint,
the wire bond bumps further spacing the micro-machined semiconductor device from the first surface, the wire bond bumps further arranged around the active area, the wire bond bumps formed from a metal; and

a plurality of solder spheres mounted to the ball pads by a second reflowed solder paste.

26. (new) The semiconductor package according to claim 25, wherein a plurality of circuit lines are located on the first surface, the circuit lines connected between the vias and the second pads.

27. (new) The semiconductor package according to claim 25, wherein the substrate does not have cavity.

28. (new) The semiconductor package according to claim 25, wherein the wire bond bumps are formed from either gold or an alloy of gold.